

APPARATUS AND METHOD FOR REAL-TIME ADJUSTING SYSTEM PERFORMANCE OF A COMPUTER

Field of the invention

5 [0001] The present invention relates to an apparatus for real-time
adjusting the system performance of a computer, and more particularly, to
an apparatus fabricated on the motherboard of the computer for
monitoring the operating state of each device on the motherboard and
automatically adjusting power sources supplied to the device, to optimize
10 the system performance.

Background of the invention

[0002] With the continuing advances and developments of electrical
15 manufactures, the multimedia computers in new generation with high
image and audio quality are widely used and more popular. The
expenditure enhancement for computers also causes the popularization
and vigorous development of related industry. As well known, the system
performance of a computer is decided mainly by the motherboard and
20 those devices, such as CPU, RAM, chip sets, etc., fabricated thereon.

[0003] For instance, the new generation of CPU has more fine and
complicated internal frame fabricated so as to provide higher operating
frequency and multiple powerful computing functions. And the new
25 generation of PC133 and PC150 DRAMs are introduced to promote the
ability to deal with multi-media data of personal computers due to its
enlarged memory space. Except for the CPU and memory, other devices,

such as south and north bridge chips, AGP cards, net cards, and modem cards, are manufactured with more complicated structures and powerful functions, to satisfy the requirements of consumers.

5 [0004] However, for the various devices with the more complicated structures therein, how to integrate effectively these devices for further promoting system performance has become an important issue. Actually, when a computer system is operated, the devices on the motherboard usually have different loadings. For example, when the executing program
10 needs a large number of computing procedures, the CPU will be involved in a busy state; and when the executing program centers on transferring and processing of graphical data, the AGP card will be kept in a busy state.

[0005] Namely, when a program is executed, sometimes the CPU or
15 memory device is busy, sometimes the peripheral devices mounted on the PCI slots are busy, and sometimes for a lot of devices there is nothing to handle. Therefore, if the all devices can be integrated effectively and the system source such as power or bandwidth can be allotted to these devices according to their actual operating states, the system performance
20 of the computer will be further promoted. For instance, if the task of executed programs centers on the operation of the memory device, the source supplied to the memory device can be increased; and if there is nothing to deal with for the CPU, the operating rate of the CPU can be slowed down so as to reduce power consumption and promote system
25 performance.

[0006] Though in current producing lines, the manufacturers usually preset the operating rate and voltage of each device and predetermine the optimal parameters of system performance according to experiences and

trade-off. However, when the computer is in operation, the constant optimal parameters can not be real-time adjusted to have the system source redeployed basing the operating state of each device. Hence, in practice, the preset priority for each device to share the source is usually different
5 with the actual need of the computer system according to the real operating state of each device. In other words, the system performance can not be real-time optimized to fit with in the actual condition. And the computer system will consume more power and reduce the lifetime of devices.

10 Summary of the Invention

[0007] It is therefore an objective of the present invention to provide a real-time adjusting apparatus fabricated on the motherboard of the computer, to monitor and adjust the operating state of each device for optimizing the system performance.

15 [0008] The apparatus comprises a plurality of performance monitor means and a performance control chip. The performance monitor means are connected separately to the corresponding one of bus lines applied to connect devices mounted on the motherboard, for monitoring the
20 operating state of each device. The performance control chip is connected separately to the devices and responsive to the signals from the performance monitor means, so as to ascertain the operating rate of each device is busy or not and to adjust the operating rate of the devices.

25 [0009] The data flow rate can be the data access times or commands passing through the bus line per unit time. And, the bus lines comprise a

PCI bus line connected between a south bridge chip and PCI slots, an AGP bus line connected between a north bridge chip and an AGP slot, a memory bus line connected between the north bridge chip and a memory device, and a CPU bus line connected between a CPU and the north
5 bridge chip. Besides, the devices connected with the performance control chip comprise the CPU, the north bridge chip, the south bridge chip, the AGP slot, the PCI slots and motherboard power supply.

Brief Description of the Drawings

10 [0010] The invention can be more fully understood by reading the following detailed description of the preferred embodiments, with reference made to the accompanying drawings, wherein:

[0011] FIGURE 1 is a schematic view showing the adjusting apparatus fabricated on the motherboard; and

15 [0012] FIGURE 2 is a flow chart showing the method for adjusting the system performance of the computer according to the present invention.

Detailed Description of the Preferred Embodiment

[0013] Please refer to FIGURE 1, the motherboard 10 provided by the
20 present invention is illustrated. As shown in the FIGURE, the devices fabricated on the motherboard 10 comprise a CPU 12, a north bridge chip 14 and a south bridge chip 16. The CPU 12 is used to execute various computing functions of the computer system. As to the north bridge chip 14 and the south bridge chip 16 are applied to transfer commands from
25 the CPU 12 to other devices on the motherboard 10 for executing, or to

send messages from various device back to the CPU 12.

[0014] The devices fabricated on the motherboard 10 further comprise a memory 18, an AGP slot 20, three pieces of PCI slots 22 and a motherboard power supply 24. The memory 18 is fabricated below the north bridge chip 14 for storing the data and programs in use of the computer system, The AGP slot 20 is applied to mount an AGP card thereon so as to handle image data fast and perfectly. As to the PCI slots 22 can be used to connect some extra peripheral devices such as net cards, modem cards, and so on. Besides, the motherboard power supply 24 above the north bridge chip 14 and the CPU 12 is applied to provide electrical power to each device on the motherboard 10. A large number of bus lines are also fabricated on the motherboard 10 for connecting those devices and slots.

[0015] For real-time monitoring the operating state of each device on the motherboard and optimally allotting whole system source to supply the devices, an apparatus for automatically adjusting the system performance disclosed by the present invention is fabricated on the motherboard 10. This apparatus, as shown in FIGURE 1, comprises a plurality of performance monitor means 26 and a performance control chip 28. Each performance monitor means 26 is connected to one selected bus line, so as to monitor the operating state of the device which is connected to the selected bus line by counting the actual flow rate of data transferred through the selected bus line. In general, the data

access cycles or commands transferred through the selected bus line per unit time can be introduced to show the operating state of the selected device.

5 [0016] For example, a performance monitor means 26 is connected to the bus line which is applied to connect the south bridge chip 16 and the PCI slot 22, so as to monitor the actual data flow rate through this bus line for ascertaining the operating state of the peripheral device mounted on the PCI slot 22; or a performance monitor means 26 is connected to
10 the bus line between the north bridge chip 14 and the AGP slot 20 for monitoring the actual operating state of the AGP card. Similarly, another performance monitor means 26 can be connected to the memory bus line between the north bridge chip 14 and the memory 18 for monitoring the actual flow rate there through, or can be connected to the CPU bus line
15 between the CPU 12 and the north bridge chip 14 to monitor the operating state of the CPU 12.

[0017] As to the performance control chip 28 is connected separately to each device on the motherboard 10, to compare the operating state of
20 each device according to the flow rate provided by the performance monitor means 26. Then, the performance control chip 28 can redeploy the system source shared by each device, to adjust the operating rate of each device for promoting the whole system performance of the motherboard 10. As shown in FIGURE 1, the performance control chip 28
25 is connected to each performance monitor means 26 via circuits defined

on the motherboard 10 to receive the data flow rate of the selected device. Besides, the performance control chip 28 is also connected individually to the CPU 12, the north bridge chip 14, the south bridge chip 16, the AGP slot 20, the PCI slot 22 and the power supply 24 via the bus lines, for
5 comparing and ascertaining the operating state of each device according to the information provided by the performance monitor means 26, and then real-time performing the adjustments.

[0018] In a preferred embodiment, the performance monitor means 26
10 comprises a counter for counting the number of times of transferring commands or accessing data through one selected bus line per unit time. For instance, when the unit time is set to be 100 ms, then the performance monitor means 26 can measure the flow times in the period of 100 ms, and send the flow rate to the performance control chip 28. As
15 to the performance control chip 28 comprises a comparator and a register. The comparator can compare the actual flow rate provided by the performance monitor means 26 with the predetermined value stored in the register. When the flow rate of one selected device on the motherboard 10 exceeds its predetermined value, the selected device will
20 be ascertained to be in a busy state. For example, if the predetermined value of one peripheral device mounted on the PCI slot is set to be 3000 times per 100 ms, this device will be ascertained to be busy when its flow rate measured by the performance monitor device 26 is higher than 3000 times/100 ms.

25

[0019] After deciding the operating state of each device on the motherboard, the performance control chip 28 will send control signals via a timing control circuit to adjust the operating rate of each device. Namely, the operating rate of each device can be altered by adjusting the clock signals of the device. When one device is in the busy state, the clock signal of this device will be adjusted to increase its operating rate; on the contrary, when the actual flow rate of the device is below the predetermined value stored in the register of the performance control chip 28, the device will be ascertained to be not busy, thereby adjusting its clock signal to lower operating rate.

[0020] Besides, the performance control chip 28 can also send control signals to the north bridge chip 14 or the south bridge chip 16, to alter default configurations stored in the register of the north bridge chip 14 or the south bridge chip 16, for readjusting the priority of each device to share the system source. Generally, according to the default configurations set at the time the motherboard is manufactured, the priority of the device to share the system source has the sequence of CPU (1st) → AGP card (2nd) → peripheral devices mounted on the PCI slots (3rd). However, by introducing the apparatus for adjusting the system performance disclosed by the present invention, the sequence of the priority to share the system source can be readjusted according to the flow rates of the devices measured by the performance monitor means 26. For instance, when the AGP card is busy and the CPU is not busy, the performance control chip 28 will promote the priority of the AGP device,

thereby providing more system source for the AGP device.

[0021] Except readjusting the priority sequence of devices on the motherboard, the performance control chip 28 can also redistribute the system source by adjusting the bandwidth of each device. For example, when one device is busy, the performance control chip 28 will send a control signal to increase the data access cycles per unit time of the device. By resetting the bandwidth of each device on the motherboard, the operating rate of the device in the busy state can be increased by providing more system source, while the operating rate of the device which is not busy can be decreased by reducing the system source supplied thereto.

[0022] Besides, the computer system also can be optimized by adjusting the power supplied to each device because the performance control chip 28 is connected to the motherboard power supply 24. For example, when one device is busy, the voltage applied to this device can be increased under the specification to promote the operating rate of the device. On the other hand, when some device is not busy, the operating voltage applied to the device can be decreased to lower its operating rate. Thus, the whole system power can be used more effectively, so as to reduce power consumption and prolong the lifetime of devices.

[0023] The present invention also provides a method for automatically adjusting the computer system. As shown in FIGURE2, the flow chart

according to the method is illustrated as follows: (1) executing a program to make one selected device operate in a busy state (step 50); (2) measuring the data flow rate of the selected device in the busy state (step 52); (3) defining a predetermined flow rate of the selected device to indicate the selected device is busy (step 54) and storing the predetermined values in the register of the performance control chip 28; (4) repeating the above steps (1)~(3) to define the predetermined flow rates of all devices fabricated on the motherboard; (5) after determining the default flow rates of all devices, measuring the actual data flow rates of selected devices on the motherboard (step 56); (6) when the actual data flow rate of one selected device exceeds its predetermined value (step 58), promoting the operating rate of the device (step 60); (7) on the contrary, when the data flow rate of the device is less than its predetermined value, reducing the operating rate of the device (step 60).

15

[0024] The present invention has considerable advantages: (1) by introducing the performance monitor means for monitoring each device on the motherboard, the system source can be real-time redeployed according to the operating state of each device, thereby optimizing the whole system performance of the computer; (2) the computer system can automatically adjust the operating rate of each device according to requirement of the executed program, so the operating rate of the device which is not busy can be lowered, thereby reducing the operating noise of the computer and decreasing the power consumption; (3) because the computer system can real-time optimize the allotment of the system

25

source, the computer system will has better operation efficiency; (4) and when the computer system is under lower loading condition, the power source can be saved in advance.

5 [0025] The invention has been described using exemplary preferred embodiments. However, it is to be understood that the scope of the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications aid similar arrangements. The scope of the claims, therefore, should be accorded the broadest
10 interpretation so as to encompass all such modifications and similar arrangements.